## AMENDMENTS TO THE SPECIFICATION

Please amend the specification as shown below.

Please amend the paragraph beginning on page 9, line 12, with the following amended paragraph:

As [one of measures] <u>a measure</u> against degradation during data retention of such a nonvolatile memory, refresh is considered.

Please amend the paragraph beginning on page 31, line 24 and continuing on page 32 with the following amended paragraph:

In addition, an inverter IV11 and a switch Q1 formed by a FET (P-channel MOS transistor) are provided within the memory chip 11b. The switch Q1 is formed on a power supply path for supplying operating power from the power supply terminal 48 to a memory core 15c during standby of the memory chip 11b.

Please amend the paragraph beginning on page 32, line 6, with the following amended paragraph:

The power-on pulse Sp is inputted from the control circuit 13b to a gate of the switch Q1 after being inverted by the inverter IV11. Thus, the switch Q1 is turned on in response to the power-on pulse Sp to supply operating power to the memory core 15c.

Please amend the paragraph beginning on page 32, line 11, with the following amended paragraph:

47

The memory core 15c having a memory cell array formed by a ferroelectric memory includes therewithin the power-on refresh signal generating circuit 21 as described with reference to FIG. 5.

Please amend the paragraph beginning on page 32, line 15, with the following amended paragraph:

Thus, when the switch Q1 is turned on and power is supplied to the memory core 15c, the power-on refresh signal generating circuit 21 generates an event pulse EP for starting refresh. In response to the event pulse EP, a refresh operation corresponding to the ROW address signal Ad from the control circuit 13b is performed.

Please amend the paragraph beginning on page 38, line 14, with the following amended paragraph:

Thus, part of <u>a</u> charge within the memory core 15c is stored to be reused at a next time of turning on power. Therefore, the third embodiment can further reduce current consumption as compared with the first and second embodiments, which interrupt only the power.